Enrollment No: _____ Exam Seat No:_____

C.U.SHAH UNIVERSITY

Summer Examination-2019

Subject Name : Advanced Computer Architecture

Subject Code : 4TE08ACA1 Branch: B.Tech (IT)

Semester : 8 Date : 15/04/2019 Time : 10:30 To 01:30 Marks : 70

Instructions:

(1) Use of Programmable calculator & any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

Q-1 Attempt the following questions:

(a) Define computer architecture. **(01)**
(b) What is reservation table? **(01)**
(c) Define: Pipeline stalling. **(01)**
(d) What is vector processor? **(01)**
(e) Define: Branch prediction. **(01)**
(f) What is ILP? **(01)**
(g) Define: TLB **(01)**
(h) What do you mean by multi-core processor? **(01)**
(i) What is tightly coupled system? **(01)**
(j) Define: Dynamic scheduling. **(01)**
(k) What is multithreading? **(01)**
(l) Define: Data hazard. **(01)**
(m) What is parallel processing? **(01)**
(n) What do mean by cache miss penalty? **(01)**

Attempt any four questions from Q-2 to Q-8

Q-2 (a) Explain memory hierarchy in computer system. **(07)**
(b) Explain different techniques of Speculation-Compiler for ILP. **(07)**

Q-3 (a) Explain virtual memory technology. **(07)**
(b) Explain super scalar processor. **(07)**

Q-4 (a) Explain arithmetic pipeline design. **(07)**
(b) Explain challenges of ILP. **(07)**

Q-5 (a) Explain distributed shared memory multiprocessor. **(07)**
(b) Explain different models of memory consistency. **(07)**

Q-6 (a) Explain non-linear pipeline processor. **(07)**
(b) Explain compiler optimization to reduce the miss rate. **(07)**

Q-7 **(a)** Explain RAID with various levels. **(07)**
(b) Explain design issues of multi-core architecture. **(07)**

Q-8 **(a)** Explain design steps of I/O system. **(07)**
(b) Explain heterogeneous multi-core processors. **(07)**